

Application Serial No.: 10/780,932

**REMARKS**

The Examiner is thanked for the thorough examination of this application. The Office has tentatively rejected all claims. Applicant has amended claims herein and for at least the reasons discussed below, Applicant requests reconsideration and withdrawal of the rejections.

**Rejections Under 35 U.S.C. 102(b)**

Claims 1-8 were rejected under 35 U.S.C. 102(b) as allegedly anticipated by the acknowledged prior art of Figs. 1-2E. In forming this rejection, the Office Action alleged that "the prior art disclose each ITO wiring 162 being isolated and enclosed by each opening (the openings between the element 151 and 152; see Fig.1 and Fig.2E) of the passivation structure (151 and 152) respectively".

As amended, claim 1 recites:

1. An interconnect structure, comprising:
  - a substrate;
  - a plurality of first metal lines disposed on the substrate;
  - a first insulating layer disposed on the substrate, covering the plurality of first metal lines;
  - a plurality of second metal lines disposed on the first insulating layer;
  - a second insulating layer covering the plurality of second metal lines;
  - a plurality of ITO (indium tin oxide) wirings electrically connecting the plurality of first and second metal lines respectively; and
  - a passivation structure disposed on the second insulating layer, *having surrounding walls to isolate each of the ITO wirings.*

*(Emphasis Added)*

It is clear that the interconnect structure of claim 1 comprises *a passivation structure disposed on the second insulating layer, having surrounding walls to isolate each of the ITO wirings.*

In contrast to the claimed embodiments, page 2, lines 10-20 of the specification (regarding the AAPA) states:

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FIG. 1 is a top view of part of a peripheral circuit for ESD protection in a non-display area of a TFT array substrate. Three parallel metal lines 110, e.g. gate metal lines, opposite to three parallel metal lines 130, e.g. source/drain metal lines, are disposed on the non-display area of a TFT array substrate 100. Each metal line 110 is bridged to the opposite metal line 130, utilizing ITO layers 162 as the wirings. Two passivation layers 151 and 152, parallel to each other, are disposed on opposite sides of the bridging regions, *with a trench therebetween exposing the ITO wirings 162.*

It is, therefore, clear that the AAPA teaches *a trench (opening) between two passivation layers 151 and 152 exposing the ITO wirings 162.* The Office Action refers to the opening between 160 and 160' in FIG. 1 as one of the openings in claim 1, and assumes that each ITO wiring 162 being isolated and surrounded by the opening between 160 and 160'. However, in FIG. 1, the ITO wiring 162 indeed is not isolated by the opening between 160 and 160', as in the opening, ITO wirings 162 can connect with each other. Consequently, the admitted prior art of Applicant's disclosure does not disclose *a passivation structure disposed on the second insulating layer, having surrounding walls to isolate each of the ITO wirings*, as specifically recited in amended claim 1.

For at least this reason, claim 1 defines over the prior art of record. Insofar as claims 2-7 depend on claim 1, claims 2-7 are also allowable.

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No fee is believed to be due in connection with this amendment and response. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,



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